



STIC Search Report

EIC 2800

STIC Database Tracking Number: 140659

**TO: Andrew Tran
Location: JEF- 7A71
Art Unit : 2824
Friday, December 17, 2004**

Case Serial Number: 09/134897

**From: Darcy Bates
Location: EIC 2800
JEF- 4B68
Phone: 571-272-2540**

darcy.bates@uspto.gov

Search Notes

**08/308,534
Re: ~~09/134,897~~ US 5,570,315**

Attached are search results.

**No U. S. litigation was found in searches of
Lexis-Nexis and Questel-Orbit databases.**

**If more searching or explanation is needed, please let
me know.**

**Thanks,
Darcy Bates**

Litigation involving patent 5,570,315

Click on the docket number to view the docket.
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Terms: **patno=5570315** ([Edit Search](#))

308534 (08) 5570315 October 29, 1996

UNITED STATES PATENT AND TRADEMARK OFFICE GRANTED PATENT

5570315

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October 29, 1996

Multi-state EEPROM having write-verify control circuit

REISSUE: Reissue Application filed Aug. 17, 1998 (O.G. Jan. 19, 1999) Ex. Gp.: 2511; Re. S.N. 09/134,897, (O.G. January 19, 1999)

INVENTOR: Tanaka, Tomoharu, Yokohama, JP; Hemink, Gertjan, Kawasaki, JP

APPL-NO: 308534 (08)

FILED-DATE: September 21, 1994

GRANTED-DATE: October 29, 1996

PRIORITY: September 21, 1993 - 5-234767, Japan (JP); December 13, 1993 - 5-311732, Japan (JP)

ASSIGNEE-AT-ISSUE: Kabushiki Kaisha Toshiba, Kawasaki, JP

ASSIGNEE-AFTER-ISSUE: September 21, 1994 - ASSIGNMENT OF ASSIGNORS INTEREST (SEE DOCUMENT FOR DETAILS)., KABUSHIKI KAISHA TOSHIBA 72 HORIKAWA- CHO, SAIWAI-KU, KAWASAKI-SHI JAPAN, Reel and Frame Number: 007137/0465

LEGAL-REP: Oblon, Spivak, McClelland, Maier & Neustadt, P.C.

PUB-TYPE: October 29, 1996 - Utility Patent having no previously published pre-grant publication (A)

PUB-COUNTRY: United States (US)

US-MAIN-CL: 365#185.22

US-ADDL-CL: 365#185.03, 365#185.12, 365#185.17, 365#185.18, 365#185.21

CL: 365

SEARCH-FLD: 365#185, 365#900, 365#168, 365#184, 365#45, 365#189.05, 365#238.5, 365#185.03, 365#185.12, 365#185.17, 365#185.18, 365#185.21, 365#185.22

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patno=5570315

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Syntax Definition

<u>and</u>	and
<u>or</u>	or
<u>w/N</u>	within N words
<u>not w/N</u>	not within N words
<u>pre /N</u>	precedes by N words
<u>w/p</u>	in same paragraph
<u>not w/p</u>	not in same paragraph
<u>w/seg</u>	in same segment
<u>not w/seg</u>	not in same segment
<u>w/s</u>	in same sentence
<u>not w/s</u>	not in same sentence
<u>and not</u>	and not
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not w/seg	not in same segment
w/s	in same sentence
not w/s	not in same sentence
and not	and not

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<u>not w/p</u>	not in same paragraph
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<u>and not</u>	and not
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w/s	in same sentence
not w/s	not in same sentence
and not	and not
View Search Command	

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Selected file: PLUSPAT

Search statement 1

Query/Command : us5570315/pn

** SS 1: Results 1

Search statement 2

Query/Command : prt fu legalall max

1 / 1 PLUSPAT - @QUESTEL-ORBIT - image
PN - US5570315 A 19961029 [US5570315]
TI - (A) Multi-state EEPROM having write-verify control circuit
PA - (A) TOKYO SHIBAURA ELECTRIC CO (JP)
PAO - Kabushiki Kaisha Toshiba, Kawasaki [JP]
IN - (A) HEMINK GERTJAN (JP); TANAKA TOMOHARU (JP)
AP - US30853494 19940921 [1994US-0308534]
PR - JP23476793 19930921 [1993JP-0234767]
JP31173293 19931213 [1993JP-0311732]
IC - (A) G11C-016/04
EC - G11C-011/56D
G11C-011/56D2
PCL - ORIGINAL (O) : 365185220; CROSS-REFERENCE (X) : 365185030
365185120 365185170 365185180 365185210
DT - Corresponding document
CT - US5218569; US5394362; DE4232025
STG - (A) United States patent
AB - An EEPROM having a memory cell array in which electrically programmable memory cells are arranged in a matrix and each of the memory cells has three storage states, includes a plurality of data circuits for temporarily storing data for controlling write operation states of the plurality of memory cells, a write circuit for performing a write operation in accordance with the contents of the data circuits respectively corresponding to the memory cells, a write verify circuit for confirming states of the memory cells set upon the write operation, and a data updating circuit for updating the contents of the data circuits such that a rewrite operation is performed to only a memory cell, in which data is not sufficiently written, on the basis of the contents of the data circuits and the states of the memory cells set upon the write operation. A write operation, a write verify operation, and a data circuit content updating operation based on the contents of the data circuits are repeatedly performed until the memory cells are set in predetermined written states.

1 / 1 LGST - @EPO
PN - US5570315 A 19961029 [US5570315]
AP - US30853494 19940921 [1994US-0308534]
ACT - 19940921 US/AS02-A
ASSIGNMENT OF ASSIGNOR'S INTEREST
OWNER: KABUSHIKI KAISHA TOSHIBA 72 HORIKAWA-CHO, SAIWAI-K;
EFFECTIVE DATE: 19940908

19940921 US/AS02-A
ASSIGNMENT OF ASSIGNOR'S INTEREST
OWNER: TANAKA, TOMOHARU; EFFECTIVE DATE: 19940908

19940921 US/AS02-A
ASSIGNMENT OF ASSIGNOR'S INTEREST
OWNER: HEMINK, GERTJAN; EFFECTIVE DATE: 19940908

19990119 US/RF-A
REISSUE APPLICATION FILED
EFFECTIVE DATE: 19980817

UP - 2003-22

1 / 1 CRXX - @CLAIMS/RRX
AN - 2777437
PN - 5,570,315 A 19961029 [US5570315]
PA - Toshiba Corp JP
PT - E (Electrical)
ACT - 19980817 REISSUE REQUESTED
Issue Date of O.G.: 19990119
Reissue Request Number: 09/134897
Examination Group responsible for Reissue process: 2511

UP - 2000-05
UACT- 2000-02-01

Search statement 2

Query/Command : fam us5570315/pn

1 Patent Groups
** SS 2: Results 6

Search statement 3

Query/Command : famstate nonstop

1 / 6 PLUSPAT - @QUESTEL-ORBIT
PN - DE4433721 A1 19950323 [DE4433721]
STG - (A1) Doc. Laid open (First publication)
TI - (A1) Non-volatile semiconductor memory arrangement
OTI - (A1) Nichtflüchtige Halbleiterspeicheranordnung
PA - (A1) TOSHIBA KAWASAKI KK (JP)
IN - (A1) HEMINK GERTJAN (JP); TANAKA TOMOHARU (JP)
IC - (A1) G11C-016/06
PN2 - DE4433721 C2 20001207 [DE4433721]
STG2- (C2) Patent Specification (Second publication)
OTI2- (C2) Nichtflüchtige Halbleiterspeicheranordnung
PA2 - (C2) TOSHIBA KAWASAKI KK (JP)

IN2 - (C2) HEMINK GERTJAN (JP); TANAKA TOMOHARU (JP)
IC2 - (C2) G11C-016/06
AP - DE4433721 19940921 [1994DE-4433721]
PR - JP23476793 19930921 [1993JP-0234767]
JP31173293 19931213 [1993JP-0311732]
EC - G11C-011/56D
G11C-011/56D2
DT - Basic

1 / 1 LEGALI - ©EPO
PN - DE4433721 A1 19950323 [DE4433721]DE4433721 C2 20001207 [DE4433721]
AP - DE4433721 19940921 [1994DE-4433721]
ACTE- 19950323 DE/OP8-A [+]
REQUEST FOR EXAMINATION AS TO PARAGRAPH 44 PATENT LAW

20001207 DE/D2-A [+]
GRANT AFTER EXAMINATION

20010531 DE/8364-A [+]
NO OPPOSITION DURING TERM OF OPPOSITION
UP - 2003-22

2 / 6 PLUSPAT - ©QUESTEL-ORBIT - image
PN - JP7093979 A 19950407 [JP07093979]
STG - (A) Doc. Laid open to publ. Inspec.
TI - (A) NONVOLATILE SEMICONDUCTOR MEMORY DEVICE
PA - (A) TOKYO SHIBAURA ELECTRIC CO
PA0 - (A) TOSHIBA CORP
IN - (A) TANAKA TOMOHARU
IC - (A) G11C-016/04 G11C-016/06
PN2 - JP3226677 B2 20011105 [JP3226677]
STG2- (B2) Grant. Pat. With A from 2500000 on
IC2 - (B2) G11C-016/02 G11C-016/06
AP - JP23476793 19930921 [1993JP-0234767]
PR - JP23476793 19930921 [1993JP-0234767]
EC - G11C-011/56D
G11C-011/56D2

3 / 6 PLUSPAT - ©QUESTEL-ORBIT - image
PN - JP7161852 A 19950623 [JP07161852]
STG - (A) Doc. Laid open to publ. Inspec.
TI - (A) NONVOLATILE SEMICONDUCTOR MEMORY
PA - (A) TOKYO SHIBAURA ELECTRIC CO
PA0 - (A) TOSHIBA CORP
IN - (A) HEMINKU GERUTOYAN; TANAKA TOMOHARU
IC - (A) G11C-016/04 G11C-016/06 H01L-021/8247 H01L-029/788 H01L-029/792
PN2 - JP3181454 B2 20010703 [JP3181454]
STG2- (B2) Grant. Pat. With A from 2500000 on
IC2 - (B2) G11C-016/02 H01L-021/8247 H01L-027/115 H01L-029/788
AP - JP31173293 19931213 [1993JP-0311732]
PR - JP31173293 19931213 [1993JP-0311732]
EC - G11C-011/56D
G11C-011/56D2

4 / 6 PLUSPAT - @QUESTEL-ORBIT
PN - KR169267 B1 19990201 [KR-169267]
STG - (B1) Examined pat. App. (2nd pub.) B5
TI - (B1) NONVOLATILE SEMICONDUCTOR MEMORY DEVICE
PA - (B1) TOKYO SHIBAURA ELECTRIC CO (JP)
IN - (B1) TANAKA TOMOHARU (JP); HEMINK GERTJAN (JP)
IC - (B1) G11C-016/02
AP - KR9423567 19940916 [1994KR-0023567]
PR - JP23476793 19930921 [1993JP-0234767]
JP31173293 19931213 [1993JP-0311732]

5 / 6 PLUSPAT - @QUESTEL-ORBIT - image
PN - US5570315 A 19961029 [US5570315]
STG - (A) United States patent
TI - (A) Multi-state EEPROM having write-verify control circuit
PA - (A) TOKYO SHIBAURA ELECTRIC CO (JP)
PAO - Kabushiki Kaisha Toshiba, Kawasaki [JP]
IN - (A) HEMINK GERTJAN (JP); TANAKA TOMOHARU (JP)
IC - (A) G11C-016/04
AP - US30853494 19940921 [1994US-0308534]
PR - JP23476793 19930921 [1993JP-0234767]
JP31173293 19931213 [1993JP-0311732]
EC - G11C-011/56D
G11C-011/56D2
PCL - ORIGINAL (O) : 365185220; CROSS-REFERENCE (X) : 365185030
365185120 365185170 365185180 365185210
DT - Corresponding document

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PN - US5570315 A 19961029 [US5570315]
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OWNER: HEMINK, GERTJAN; EFFECTIVE DATE: 19940908

19990119 US/RF-A
REISSUE APPLICATION FILED
EFFECTIVE DATE: 19980817
UP - 2003-22

6 / 6 PLUSPAT - @QUESTEL-ORBIT - image
PN - US5652719 A 19970729 [US5652719]
STG - (A) United States patent
TI - (A) Nonvolatile semiconductor memory device
PA - (A) TOKYO SHIBAURA ELECTRIC CO (JP)
PAO - Kabushiki Kaisha Toshiba, Kawasaki [JP]
IN - (A) HEMINK GERTJAN (JP); TANAKA TOMOHARU (JP)
IC - (A) G11C-016/04

12/17/04

US 5,570,315

09/134897

AP - US68200996 19960716 [1996US-0682009]
PR - US68200996 19960716 [1996US-0682009]
JP23476793 19930921 [1993JP-0234767]
JP31173293 19931213 [1993JP-0311732]
US30853494 19940921 [1994US-0308534]
EC - G11C-011/56D
G11C-011/56D2
PCL - ORIGINAL (O) : 365185030; CROSS-REFERENCE (X) : 365185170
365185220
DT - Basic

Litigation involving patent 5,652,719

Click on the docket number to view the docket.
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▼ Docket ▲ ▼ Case Heading ▲ ▼ Date Filed ▲ ▼ Date Retrvd ▲

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